TPS65030EVM-162

This user's guide describes the characteristics, operation, and use of the TPS65030EVM-162 evaluation module (EVM). This EVM demonstrates the Texas Instruments TPS65030 power management IC for USB On-The-Go (USB-OTG) applications. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

The Texas Instruments TPS65030EVM-162 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS65030 power management IC for USB-OTG applications. The TPS65030 contains four regulated output voltages and operates from a 3-V to 5-V input supply. The supplied outputs provide all the necessary supply voltages for USB-OTG. The EVM has jumpers for all input pins for easy evaluation of the EN_, SW_, SLEEP, and TEST $\overline{\text{SRP}}$ inputs. A power-good output (PGood) is available for easy power supply sequencing applications. The 1-MHz charge pump design as well the 25-ball chip scale package provide a small footprint solution.

1.1 Related Documentation From Texas Instruments

TPS65030 data sheet (SLVS620)

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS65030EVM-162.

2.1 Input/Output Connector Descriptions

2.1.1 J1 —VIN

This is the positive input voltage connection to the converter. The EVM operates from any supply voltage between 3 V and 5 V. The leads to the input supply should be twisted together and kept as short as possible to minimize EMI transmission and input voltage droop.

2.1.2 J2 — GND

This is the input return connection for the input power supply.

2.1.3 J3 —VOUT1

This is the positive output voltage connection from the VBUS output. This charge pump regulator output regulates to 5 V and supplies up to 100 mA.

2.1.4 J4 — GND

This is the output ground connection for the VOUT1 charge pump.

2.1.5 J5 —VOUT2

This is the positive output voltage connection from the VOUT2 output. This charge pump regulator output regulates to 3.3 V and supplies up to 22 mA.

2.1.6 J6 — GND

This is the output ground connection for the VOUT2 charge pump and VOUT4 LDO regulators.

2.1.7 J7 —VOUT3

This is the positive output voltage connection from the VOUT3 output. This charge pump regulator output regulates to 1.5 V and supplies up to 200 mA.

2.1.8 J8 —GND

This is the output ground connection for the VOUT3 charge pump.

2.1.9 J9 —VOUT4

This is the positive output voltage connection from the VOUT4 output. This LDO regulator output regulates to 1.8 V and supplies up to 60 mA.

2.1.10 JP1 —VBUS Converter Enable

JP1 is used to enable the VBUS converter (VOUT1). Place a shunt in the ON position to turn the VBUS converter on. When the VBUS converter is enabled, VOUT1 regulates to 5 V and supplies up to 100 mA. Place a shunt in the OFF position to turn the VBUS converter off. VOUT1 is high impedance when the VBUS converter is disabled.

2.1.11 JP2 —VOUT2 and VOUT3 Converter Enable

JP2 is used to enable the VOUT2 and VOUT3 converters. Place a shunt in the ON position to turn the VOUT2 and VOUT3 converters on. When the VOUT2 and VOUT3 converters are enabled, VOUT2 regulates to 3.3 V and supplies up to 22 mA, and VOUT3 regulates to 1.5 V and supplies up to 200 mA. Place a shunt in the OFF position to turn the VOUT2 and VOUT3 converters off. VOUT2 and VOUT3 are high impedance when the converters are disabled.

2.1.12 JP3 —VOUT4 Converter Enable

JP3 is used to enable the VOUT4 LDO. Place a shunt in the ON position to turn the VOUT4 LDO on. When the VOUT4 LDO is enabled, VOUT4 regulates to 1.8 V and supplies up to 60 mA. Place a shunt in the OFF position to turn the VOUT4 LDO off. VOUT4 is high impedance when the LDO is disabled.

2.1.13 JP4 —Sleep Mode Enable

JP4 is used to enable the sleep mode feature for VOUT2, VOUT3, and VOUT4. Place a shunt in the ON position to enable sleep mode. During sleep mode, VOUT2, VOUT3, and VOUT4 are regulated using low-power LDOs. VOUT2 regulates to 3 V, VOUT3 regulates to 1.5 V and VOUT4 regulates to 1.8 V. All three outputs supply up to 100 μA. Place a shunt in the OFF position to turn the sleep mode off and return to normal operation.

2.1.14 JP5 —VOUT3 Switchover Enable

JP5 is used to enable the VOUT3 switchover function. Place a shunt in the ON position to enable the switchover function. When the switchover function is enabled, VOUT3 is powered from VBUS unless VBUS is below 4.3 V. When VBUS is less than 4.3V, VOUT3 is powered from VIN. If sleep mode is enabled, VOUT3 is powered from VIN regardless of this jumper location. Place a shunt in the OFF position to disable the VOUT3 switchover function. VOUT3 is always powered from VIN when the switchover mode is disabled.

2.1.15 JP6 – VOUT2 Switchover Enable

JP6 is used to enable the VOUT2 switchover function. Place a shunt in the ON position to enable the switchover function. When the switchover function is enabled, VOUT2 is powered from VBUS unless VBUS is below 4.3 V. In this case, VOUT2 is powered from VIN. If sleep mode is enabled, VOUT2 is powered from VIN regardless of this jumper location. Place a shunt in the OFF position to disable the VOUT2 switchover function. VOUT2 is always powered from VIN when the switchover mode is disabled.

2.1.16 JP7 — Current-Limit Selection and TEST Mode Indicator

JP7 is used for two functions. The first is to select the current-limit during start-up. Place a shunt across the jumper to select a 1-mA current limit during start-up. Remove the shunt to select a 100-mA current limit during start-up.

The second function for JP7 is signal output during test mode. If test mode is enabled, pin 1 of JP7 goes either high or low to indicate connectivity status. See the “TEST Input $\overline{\text{SRP}}$ Enable” section of the TPS65030 data sheet (SLVS620) or details on entering test mode and connectivity status indicator.

2.1.17 TP1 — Power Good Output

TP1 is used to monitor the PGood signal. TP1 goes high a minimum 3.1 ms after VOUT2, VOUT3, and VOUT4 exceed the PGood thresholds. The thresholds are 85% of the regulation voltage for VOUT2, and 90% of the regulation voltage for VOUT3 and VOUT4. The PGOOD pin goes low if one of these outputs falls below its threshold. Outputs that are disabled are ignored by the PGood circuitry.

2.2 Setup

1. Configure JP1 to enable or disable VBUS as desired
2. Configure JP2 to enable or disable VOUT2 and VOUT3 as desired
3. Configure JP3 to enable or disable VOUT4 as desired
4. Configure JP4 to enable or disable sleep mode as desired
5. Configure JP5 to enable or disable VOUT3 switchover mode as desired
6. Configure JP6 to enable or disable VOUT2 switchover mode as desired
7. Configure JP7 to set the start-up current-limit as desired
8. Connect the input voltage return to J2.
9. Connect the positive input voltage to J1.
10. Turn on input voltage.
11. The output voltages that were enabled by JP1, JP2, and JP3 are available.

3 Board Layout

This section provides the TPS65030EVM-162 board layout and illustrations.

3.1 Layout

Figure 1 through Figure 5 show the board layout for the TPS65030EVM-162 PCB.

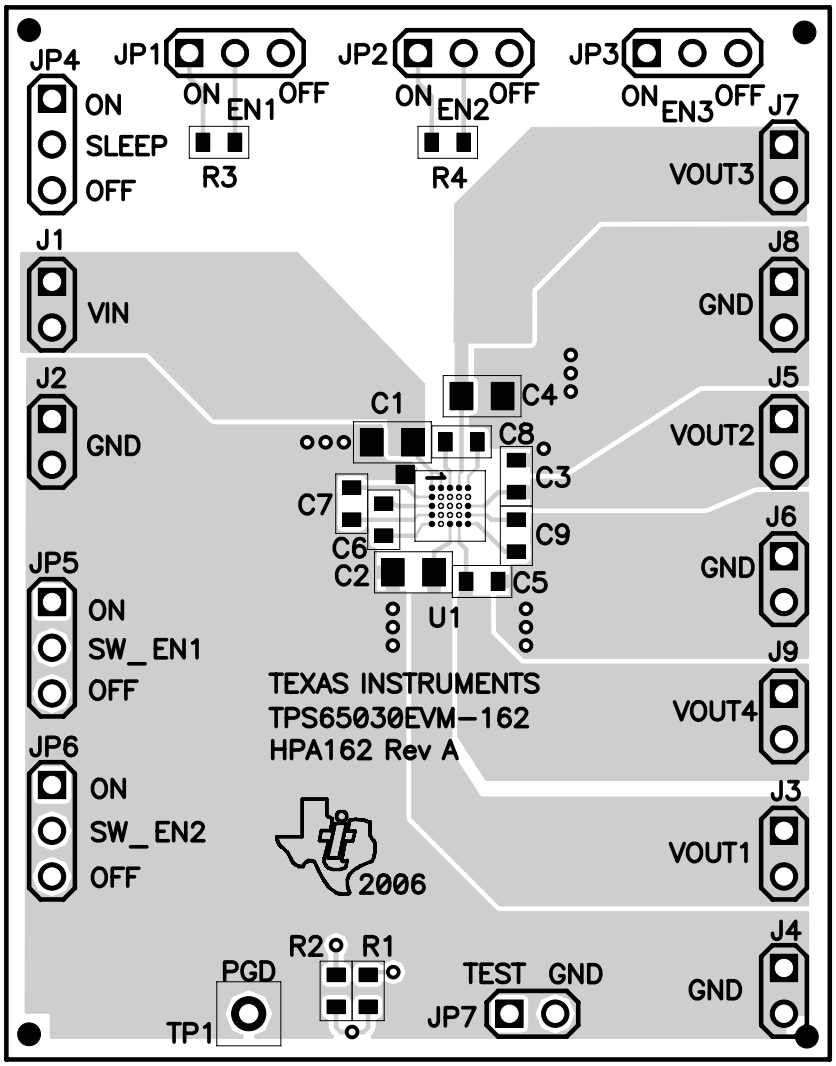

Figure 1. Assembly Layer

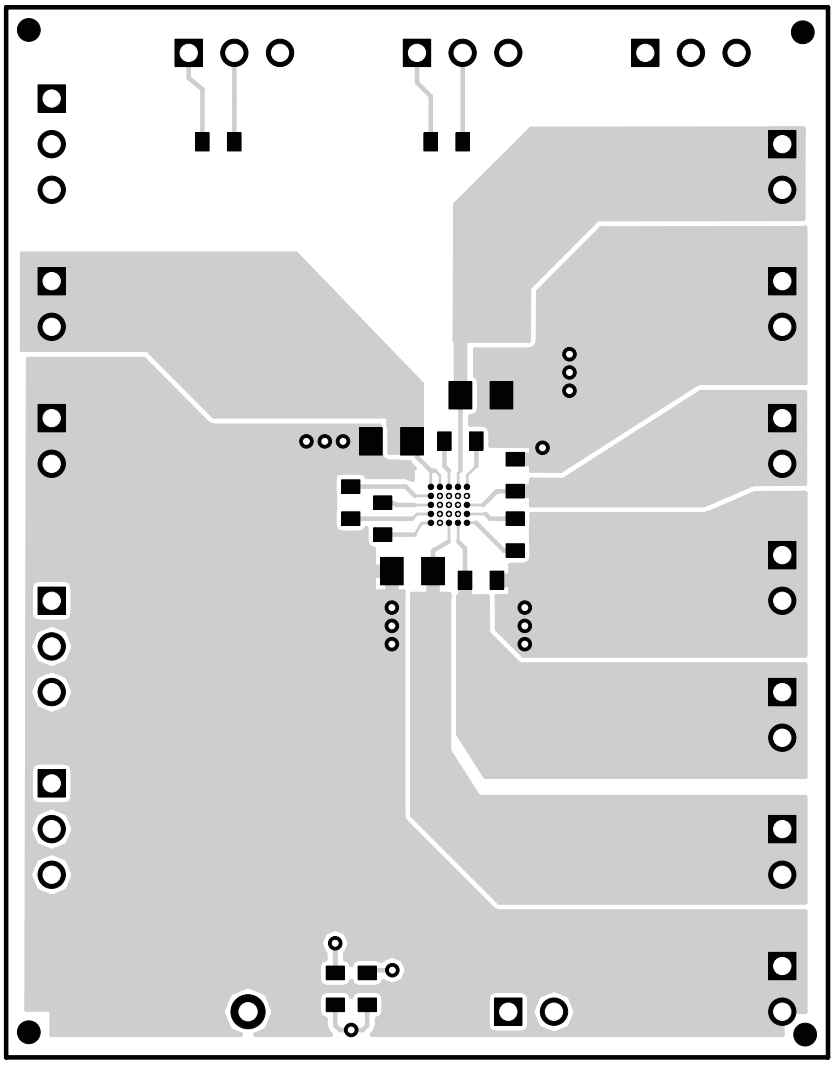

Figure 2. Top Layer Routing

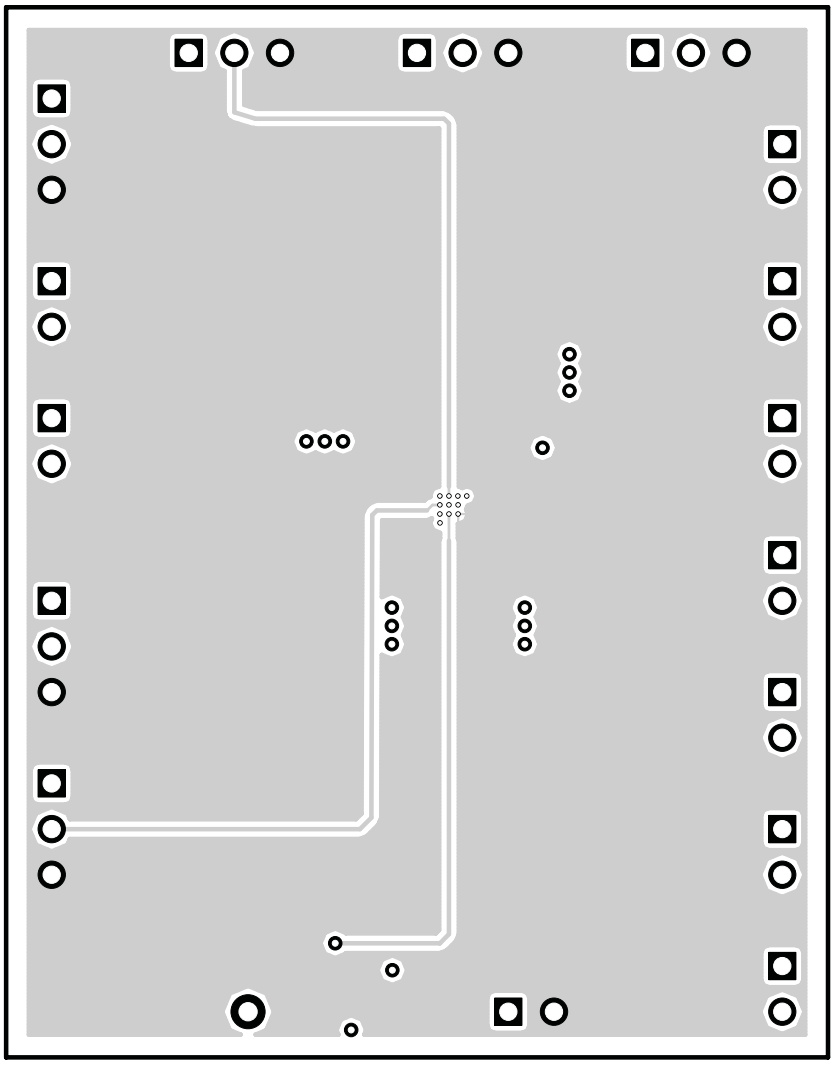

Figure 3. Layer 2 Routing

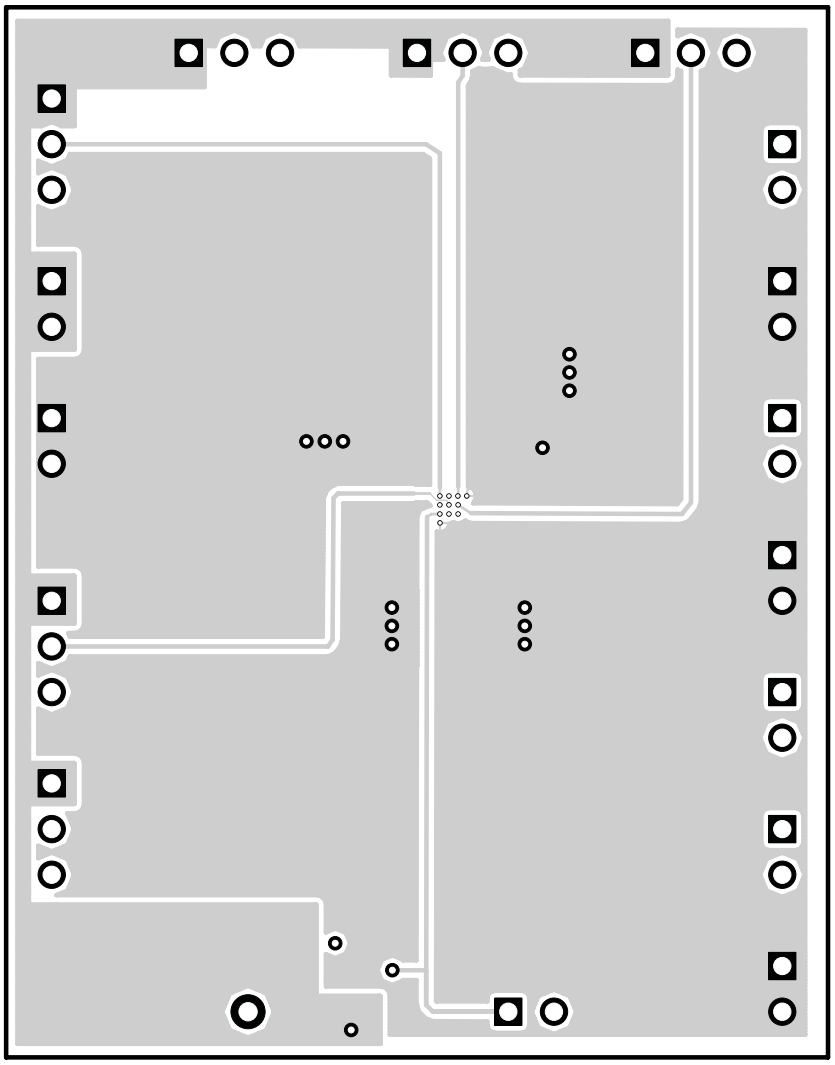

Figure 4. Layer 3 Routing

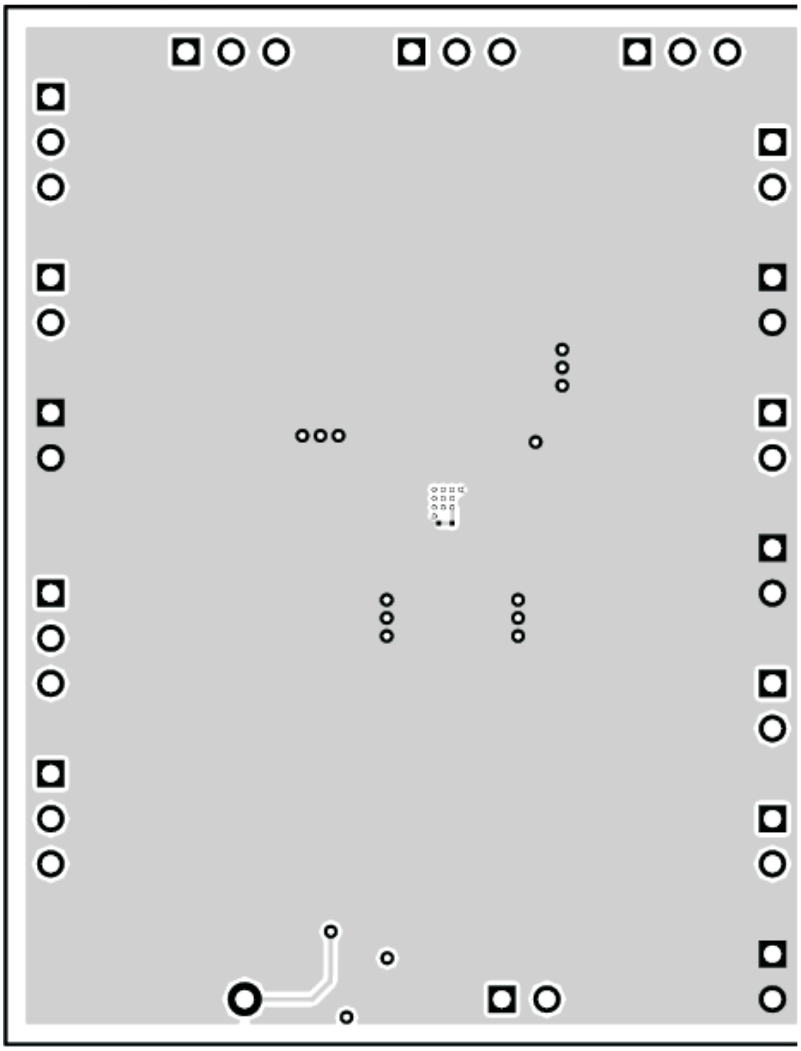

Figure 5. Bottom Layer Routing

4 Schematic and Bill of Materials

This section provides the TPS65030EVM-162 schematic and bill of materials.

4.1 Schematic

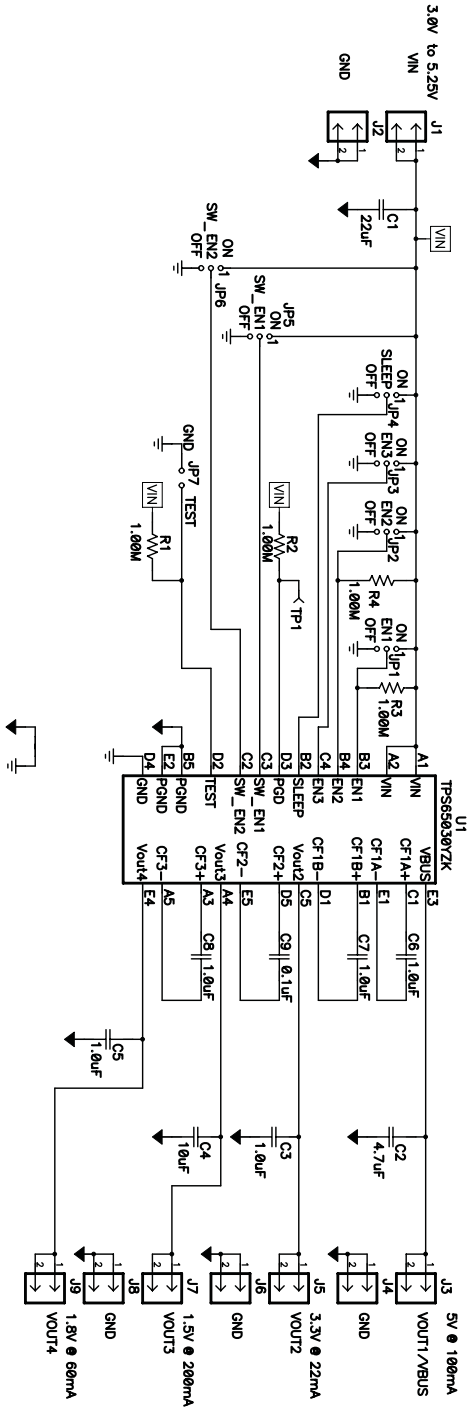

Figure 6. TPS65030EVM-162 Schematic

4.2 Bill of Materials

Table 1. TPS65030EVM-162 Bill of Materials

COUNT	Ref Des	Value	Description	Size	Part Number	MFR
1	C1	22uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J226M	TDK
1	C2	4.7µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	C2012X5R0J475K	TDK
5	C3, C5–C8	1.0µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C105K	TDK
1	C4	10µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	C2012X5R0J106M	TDK
1	C9	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	C1608X7R1H104K	TDK
9	J1–J9		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
6	JP1–JP6		Header, 3 pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
1	JP7		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
4	R1–R4	1.00M	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	TP1		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
1	U1		IC, Power Management for USB-OTG	BGA-25	TPS65030YZK	TI
1	—		PCB, 2.3 In × 1.8 In × 0.062 In		HPA162	Any
7	—		Shunt, 100mil, Black	0.100	929950-00	3M

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5 V and the maximum output voltage of 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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